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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,428	03/02/2004	Ang-Sheng Lin	12539-US-PA	2427

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HUANG, DAVID S	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
11/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/708,428	LIN, ANG-SHENG	
	Examiner	Art Unit	
	David Huang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,9 and 10* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to **the foreign priority claim and oath or declaration** have been fully considered and are persuasive. The objections have been withdrawn.

2. Applicant's arguments with respect to **the drawings** have been fully considered and are persuasive. The objection of 5/18/2007 has been withdrawn.

3. Applicant's arguments with respect to **claim 3** have been fully considered and are persuasive. The objection of 5/18/2007 has been withdrawn.

4. Applicant's arguments, with respect to **claims 1, 6-8, and 10** have been fully considered and are persuasive. The 35 USC 112, 2nd paragraph rejection of 5/18/2007 has been withdrawn.

5. Applicant's arguments with respect to **claims 1-10** have been considered but are moot in view of the new ground(s) of rejection. It is noted to applicant that the previous rejections applied to claims 1-10 have been withdrawn, since one of the references, Kroebel et al. (US 2005/0190856), on which they were based is not prior art. Accordingly, this office action will not be made final.

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

7. The drawings were received on 8/16/2007. These drawings are acceptable.

8. The drawings are objected to because there are no labels for some of the blocks in Figure 3. These blocks need to have descriptive labels under 37 CFR 1.84(n) and 1.84(o);

Figure 4B has a spelling error in the two labels for "calobration".

Figure 6, in step S2, "turn of" should be changed to --turn off--; in step S4, "turn of" should be changed to --turn on-- and the space between "a" and "fter" should be deleted.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The disclosure is objected to because of the following informalities: Page 8, [0015], In the section (lines 1-2) that reads, "the quadrature module can further comprises," *comprises*

should be revised to --comprise--; Page 16, 5 lines up from the bottom, "this" should be changed to --thus--.

Appropriate correction is required.

Claim Objections

10. **Claims 1, 3, 7, and 8** are objected to because of the following informalities:

Claim 1, line 4 recites, "a current sink, coupled between the base band transconductance and the base band transconductance". This limitation is confusing since it is not immediately clear how a device can be coupled between one device. For examination on the merits, the limitation will be interpreted such that the current sink is coupled between the output and the input of the transconductance (i.e. in a feedback loop).

Claim 3, line 1 should be revised to add "wherein" following the text, "The transmitter of claim 2," to improve the language of the claim.

Claim 5, line 1 reads, "wherein offset compensation module is..." The "offset compensation module" limitation should be prefaced with the article "the".

Claim 7, line 4 was amended to read "a predetermined time interval," but claim 2, to which claim 7 depends, already recites an identical limitation. It is believed that the limitation in claim 7 refers to the same predetermined time interval, and should be revised to "the predetermined time interval".

Claim 8 is dependent on claim 7, and is objected to for the same reasons.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. **Claims 1 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (Background of the Invention, pages 1-3, and Figure 1B; hereafter AAPA) in view of Walker (US 6,154,158) and Burgin (US 6,298,096).

Regarding **claims 1 and 10**, AAPA discloses a quadrature modulator, comprising:

a base band transconductance, for converting a voltage signal into a current signal (130a and 130b, Figure 1B);

a switching pair for modulating the current signal (132a and 132b, Figure 1B).

However, the admitted prior art fails to expressly disclose (1) a current sink, coupled between the base band transconductance and the base band transconductance, for detecting a current offset of the current signal, (2) wherein when the current sink is enabled to detect the current offset of a transmitter within a predetermined time interval, the switching pair is disabled, and after the predetermined time interval lapses, the current sink is disabled and the switching pair is enabled.

With respect to item (1), Walker discloses a prior art technique for reducing direct current (DC) offset errors using an analog feedback loop 122 to measure and suppress DC offset errors (column 3, lines 47-55; Figure 4).

With respect to item (2) Burgin discloses a predistortion quadrature modulator which operates in 2 modes. The first mode, is a transmission mode in which the signals to be transmitted are modulated according to the normal operation and transmitted over a wireless link.

The second mode is a calibration mode in which no signal is being transmitted. In a TDMA system, calibration mode is made active between the transmission slots (column 4, line 61 – column 5, line 3; a predetermined time interval is implicit). In calibration mode, a determines a set of predistortion parameters for use in subsequence transmission mode operation (column 5, lines 16-20) to pre-compensate for errors introduced by circuit imperfections in the quadrature modulator (column 5, lines 25-30). This teaching is advantageous, since it improves performance by adaptively compensating for circuit imperfections before data is transmitted.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA with the prior art analog feedback loop taught by Walker since it improves performance by measuring and suppressing DC offset errors.

It would have also be obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA and Walker with the two modes of operation taught by Burgin since it improves performance by adaptively compensating for imperfections in the circuit before transmitted data can be effected in the transmission mode.

Regarding **claim 2**, AAPA discloses a transmitter, comprising:

a digital-to-analog converter module for receiving voltage signals (DAC 110a and 110b, Figure 1B);

a base band filter module, coupled to the analog converters module (112a and 112b, Figure 1B);

a quadrature module coupled to the base band filter module, for converting filtered voltage signals into current signals and then modulating the current signals (100, Figure 1B); and

a radio frequency amplifier, coupled to the quadrature module, for amplifying the modulated current signals and then transmitting amplified signals to an antenna (118, Figure 1B).

However, AAPA fails to expressly disclose (1) a current sink module, coupled to the quadrature module and enabled for intercepting the current signals to detect a current offset before the current signals are modulated;

(2) an offset compensation module, coupled between the current sink module and one of the digital-to-analog converter module, the base band filter module and the quadrature module, for compensating the current offset when the current sink module is enabled;

(3) wherein the quadrature module further comprises a base band transconductance and a switching pair, and the current sink module is arranged there between; when the current sink module is enabled within a predetermined time interval, and the switching pair is enabled after the predetermined time interval lapses.

With respect to items (1) and (2), Walker discloses a prior art technique for reducing direct current (DC) offset errors using an analog feedback loop 122 to measure *and* suppress DC offset errors (column 3, lines 47-55; Figure 4). The analog feedback circuit is connected between CDMA filters 104 and 106 and upconverting mixers 114 and 116, and feeds back to the input of the CDMA filters (Figure 4).

With respect item (3) Burgin discloses a predistortion quadrature modulator which operates in 2 modes. The first mode, is a transmission mode in which the signals to be transmitted are modulated according to the normal operation and transmitted over a wireless link. The second mode is a calibration mode in which no signal is being transmitted. In a TDMA system, calibration mode is made active between the transmission slots (column 4, line 61 –

column 5, line 3; a predetermined time interval is implicit). In calibration mode, a determines a set of predistortion parameters for use in subsequence transmission mode operation (column 5, lines 16-20) to pre-compensate for errors introduced by circuit imperfections in the quadrature modulator (column 5, lines 25-30). This teaching is advantageous, since it improves performance by adaptively compensating for circuit imperfections before data is transmitted.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA with the prior art analog feedback loop taught by Walker since it improves performance by measuring and suppressing DC offset errors.

It would have also be obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA and Walker with the two modes of operation taught by Burgin since it improves performance by adaptively compensating for imperfections in the circuit before transmitted data can be effected in the transmission mode.

Regarding **claim 3**, AAPA discloses everything claimed as applied to claim 2 above, but fails to expressly disclose when the current sink module is enabled, the switching pair is disabled.

Burgin discloses a predistortion quadrature modulator which operates in 2 modes. One of the modes is a calibration mode in which no signal is being transmitted. In a TDMA system, calibration mode is made active between the transmission slots (column 4, line 61 – column 5, line 3; a predetermined time interval is implicit). In calibration mode, a determines a set of predistortion parameters for use in subsequence transmission mode operation (column 5, lines 16-20) to pre-compensate for errors introduced by circuit imperfections in the quadrature

modulator (column 5, lines 25-30). This teaching is advantageous, since it improves performance by adaptively compensating for circuit imperfections before data is transmitted.

It would have also be obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA and Walker with the two modes of operation taught by Burgin since it improves performance by adaptively compensating for imperfections in the circuit before transmitted data can be effected in the transmission mode.

Regarding **claim 5**, AAPA disclose everything claimed as applied to claim 2 above, but fail to expressly disclose the offset compensation module is coupled between the current sink module and one of the digital-to-analog converter module, the base band filter module and the base band transconductance.

Walker discloses a prior art technique for reducing direct current (DC) offset errors using an analog feedback loop 122 to measure *and* suppress DC offset errors (column 3, lines 47-55; Figure 4). The analog feedback circuit is connected between CDMA filters 104 and 106 and upconverting mixers 114 and 116, and feeds back to the input of the CDMA filters (Figure 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA with the prior art analog feedback loop taught by Walker since it improves performance by measuring and suppressing DC offset errors.

Regarding **claim 6**, AAPA discloses everything claimed as applied to claim 2 above, and further discloses the offset compensation module is a voltage offset compensator (voltage comparator 381 and state machine 380; Figure 3; it is implicitly taught this implementation is a voltage offset compensator since it operates before the transconductance stage). Therefore, AAPA, at the very least, suggests a voltage offset compensator.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify the offset compensative module is a voltage offset compensator since in the combinations applied above, the offset compensation is applied prior to the baseband/CDMA filters, which is also prior to the transconductance stage. Therefore, the compensation is applied to voltage signals, and a voltage compensation is necessary for a voltage signal. Furthermore, AAPA teaches the use of voltage compensation is known in the prior art.

Regarding **claim 9**, AAPA fails to expressly discloses a method for detecting and compensating a current offset for a transmitter, the transmitter having a quadrature modulator including a base band transconductance stage, a switching pair and a current sink arranged there between, the method comprising:

(1) enabling the transmitter;

(2) turning on the current sink and turning off the switching pair for a predetermined time interval;

(3) compensating the current offset within the predetermined time interval; and

(4) turning off the current sink and turning on the switching pair after the predetermined time interval lapses.

Nevertheless, enabling the transmitter is inherent to operation of a transmitter, otherwise, it would not function. AAPA discloses a transmitter with a quadrature modulator including a base band transconductance (130a and 130b, Figure 1B) and a switching pair (132a and 132b). Furthermore, Walker discloses a prior art technique for reducing direct current offset errors using an analog feedback loop 122 to measure and suppress direct current offset errors (column 3, lines 47-55; Figure 4).

With respect to items (2) to (4), Burgin discloses a predistortion quadrature modulator which operates in 2 modes. The first mode, is a transmission mode in which the signals to be transmitted are modulated according to the normal operation and transmitted over a wireless link. The second mode is a calibration mode in which no signal is being transmitted. In a TDMA system, calibration mode is made active between the transmission slots (column 4, line 61 – column 5, line 3; a predetermined time interval is implicit). In calibration mode, a determines a set of predistortion parameters for use in subsequence transmission mode operation (column 5, lines 16-20) to pre-compensate for errors introduced by circuit imperfections in the quadrature modulator (column 5, lines 25-30). This teaching is advantageous, since it improves performance by adaptively compensating for circuit imperfections before data is transmitted.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA with the prior art analog feedback loop taught by Walker since it improves performance by measuring and suppressing DC offset errors.

It would have also be obvious to one of ordinary skill in the art at the time the invention was made to provide AAPA and Walker with the two modes of operation taught by Burgin since it improves performance by adaptively compensating for imperfections in the circuit before transmitted data can be effected in the transmission mode.

Allowable Subject Matter

13. **Claims 7 and 8** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Citation of Pertinent Prior Art

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Peng (US 2003/0232605) disclose a single side band transmitter in which the modulation of data and subsequence mixing of the modulated data remains in the current domain, reducing LO leakage (page 2, [0014]).

Straub et al. (US 2002/0039052) disclose a quadrature oscillator that uses transconductors to convert different clock voltage signals in to differential current clock signals to determine a phase error in the clock signals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Huang whose telephone number is (571) 270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
October 30, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER